IN THE CLAIMS

What is claimed is:

1. A semiconductor memory device, comprising:

a first bit line; and

a first memory cell including

a first storage capacitor, and

a first pass transistor coupled between the first bit line and the first storage capacitor, the first pass transistor including,

a first channel region for transferring charge between the first storage capacitor and the first bit line, and

a first top gate disposed over the first channel region, and

a first bottom gate disposed below the first channel region.

2. The semiconductor memory device of claim 1, wherein:

the first storage capacitor includes

a first storage node coupled to the first pass transistor,

a first capacitor dielectric formed on the first storage node, and

a first top plate formed over the first capacitor dielectric.

3. The semiconductor memory device of claim 2, wherein:

a second memory cell including

a second storage capacitor, and

a second pass transistor coupled between the first bit line and the second storage capacitor, the second pass transistor including,

a second channel region for transferring charge between the second storage capacitor and the first bit line,

a second top gate disposed over the second channel region, and

a second bottom gate disposed below the second channel region.

4. The semiconductor memory device of claim 3, wherein:

the second storage capacitor includes

a second storage node coupled to the second pass transistor,

a second capacitor dielectric formed on the second storage node, and

the first top plate formed over the capacitor dielectric.

5. The semiconductor memory device of claim 3, further including:

a sense amplifier coupled to the first bit line, the sense amplifier sensing the data stored in the first memory cell when the first memory cell is selected and sensing the data stored in the second memory cell when the second memory cell is selected.

6. The semiconductor memory device of claim 5, further including:

a second bit line coupled to the sense amplifier; and

the first bit line and the second bit line form a twisted bit line pair.

7. The semiconductor memory device of claim 1, further including:

a word line driver coupled to the top gate.

8. The semiconductor memory device of claim 7, further including:

a word line strapping layer coupled to the word line driver and to the top gate, the word line strapping layer being formed from a conductive material having a lower resistance than the top gate.

9. The semiconductor memory device of claim 1, further including:

a word line driver coupled to the bottom gate.

10. The semiconductor memory device of claim 1, wherein:

a word line strapping layer coupled to the word line driver and to the bottom gate, the word line strapping layer being formed from a conductive material having a lower resistance than the bottom gate.

11. A dynamic random access memory cell, comprising:

a storage capacitor; and

a pass transistor including

a source region,

a drain region,

a channel region disposed between the source region and the drain region, the channel region including a top surface and a bottom surface,

a bottom gate insulating layer formed on the bottom surface,

a bottom gate formed on the bottom gate insulating layer,

a top gate insulating layer formed on the top surface, and

a top gate formed on the top gate insulating layer.

12. The semiconductor memory device of claim 11, wherein:

the source region, drain region, and channel region are formed from a monocrystalline silicon mesa structure.

13. The semiconductor memory device of claim 12, wherein:

the monocrystalline silicon mesa structure is formed on a substrate insulating layer.

14. The semiconductor memory device of claim 13, wherein:

the substrate insulating layer includes a trench, and

the bottom gate is formed within the trench.

15. The semiconductor memory device of claim 13, wherein:

the substrate insulating layer includes silicon dioxide.

16. The semiconductor memory device of claim 11, wherein:

the bottom gate insulating layer includes thermally grown silicon dioxide.

17. The semiconductor memory device of claim 11, wherein:

the bottom gate includes polysilicon.

18. The semiconductor memory device of claim 11, wherein:

the top gate insulating layer includes thermally grown silicon dioxide.

19. The semiconductor memory device of claim 11, wherein:

the top gate includes polysilicon.

20. The semiconductor memory device of claim 19, wherein:

the top gate further includes a layer of silicide.

21. A dynamic random access memory array, comprising:

a plurality of memory cells, arranged into a plurality of generally parallel rows, each memory cell including

a pass transistor having a channel region defined by first, second third and fourth sides, the first and second sides being opposite from one another, the third and fourth sides being opposite from one another

a source region adjacent to the first side of the channel region,

a drain region adjacent to the second side of the channel region,

a first gate formed adjacent to the third side of the channel region and separated therefrom by a first gate insulating layer,

a second gate formed adjacent to the fourth side of the channel region and separated therefrom by a second gate insulating layer; and

a first word line associated with each row, each first word line being coupled to the first gates of the memory cells within its respective row

22. The dynamic random access memory array of claim 21, wherein:

the first gates of the transistors within each row are integral portions of the first word line of that row.

23. The dynamic random access memory array of claim 22, wherein:

the first word lines include polysilicon.

24. The dynamic random access memory array of claim 21, further including:

a word line strap associated with each row, each word line strap being disposed generally parallel to the first word line of its associated row, and coupled thereto by at least one strap via.

25. The dynamic random access memory array of claim 24, wherein:

the word line strap includes a metal layer.

26. The dynamic random access memory array of claim 21, further including:

a second word line associated with each row, each second word line being coupled to the second gates of the memory cells within its respective row.

27. The dynamic random access memory array of claim 26, wherein:

each first word line is coupled to the second word line of its associated row by a plurality of word line vias.

28. The dynamic random access memory array of claim 26, wherein:

a word line strap associated with each row; and

each second word line is coupled to the word line strap of its associated row by at least one strap via.

29. The dynamic random access memory array of claim 26, wherein:

the second word lines includes polysilicon.

30. The dynamic random access memory array of claim 21, wherein:

the memory cells are further arranged into a plurality of columns arranged in a generally perpendicular fashion to the rows, at least one pair of adjacent columns being separated by a strapping area;

a word line strap associated with each row, each word line strap being disposed generally parallel to the first word line of its associated row, and coupled thereto by at least one strap via; and

the first word lines and word line straps extend across the strapping area, and the strap vias are located within the strapping area.

31. The dynamic random access memory array of claim 30, further including:

a second word line associated with each row, each second word line being coupled to the second gates of the memory cells within its respective row, and further being coupled to the first word line of its respective row by a gate via, the gate via being located within the strapping area.

32. The dynamic random access memory array of claim 30, further including:

a second word line associated with each row, each second word line being coupled to the second gates of the memory cells within its respective row, and further being coupled to the word line strap of its respective row by a strap via, the strap via being located within the strapping area.